Reg.No.:												

VIVEKANANDHA COLLEGE OF ENGINEERING FOR WOMEN
[AUTONOMOUS INSTITUTION AFFILIATED TO ANNA UNIVERSITY, CHENNAI]
Elayampalayam – 637 205, Tiruchengode, Namakkal Dt., Tamil Nadu.

Question Paper Code: 60014

B.E. / B.Tech. DEGREE END-SEMESTER EXAMINATIONS – NOV. / DEC. 2024
Third Semester
Information Technology
U23IT301 – DIGITAL SYSTEMS DESIGN
(Regulation 2023)

Time: Three Hours | Maximum: 100 Marks

Answer ALL the questions

Knowledge Levels (KL)	K1 – Remembering	K3 – Applying	K5 - Evaluating
	K2 – Understanding	K4 – Analyzing	K6 - Creating

PART – A

(10 x 2 = 20 Marks)

Q.No.	Questions	Marks	KL	CO
1.	Convert the following to their binary equivalent: $(165.35)_{10}$	2	K3	CO1
2.	State & prove De-Morgan's Theorem by constructing Truth tables.	2	K1	CO1
3.	Draw the logic circuit of a Half Subtractor & brief its working philosophy.	2	K3	CO2
4.	Construct the equivalent Gray code for $[10110111]_2$.	2	K1	CO2
5.	Discern the difference between Level triggering and Edge triggering.	2	K2	CO3
6.	Find the minimum number of flip flops required to build a modulo-N counter. Justify your answer.	2	K2	CO3
7.	When does a race condition exist in an asynchronous sequential circuit?	2	K1	CO4
8.	Is it essential to have race free assignment? Justify.	2	K1	CO4
9.	Compare & contrast between Static and Dynamic RAM.	2	K2	CO5
10.	Outline the purpose of fan-in and fan-out of digital integrated circuits.	2	K1	CO5

PART – B

(5 x 13 = 65 Marks)

Q.No.			Questions	Marks	KL	CO
11.	a)	i.	Find complement of the following Boolean expression. $Y = xyz' + x'yz + z(xy+w)$	5	K3	CO1
		ii.	What are universal gates? Implement the following expression using only NOR gate and using only NAND gate. $Y = (B+C)(B+D')(A+C)$	4+4	K1	CO1
			(OR)			
	b)		Simplify the given boolean function in Product-of-Sum ()POS form using Kmap and draw the logic diagram using Only NOR gates $F(A,B,C,D) = \sum_m (0,1,4,7,8,10,12,15) + d(2,6,11,14)$.	13	K3	CO1
12.	a)		Design a full adder with neat sketch. Implement full adder with two half adders and an OR gate.	13	K2	CO2
			(OR)			
	b)	i.	Implement the following functions using 4X1 multiplexers. $F(W,X,Y,Z) = \sum_m (0,1,3,4,8,9,15)$.	9	K3	CO2
		ii.	Implement a 4 bit even parity checker.	4	K2	CO2
13.	a)		Using D Flip-Flop, design a synchronous counter that counts the sequence $000 \rightarrow 001 \rightarrow 010 \rightarrow 011 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 111 \rightarrow 000$.	13	K3	CO3
			(OR)			
	b)	i.	Realize D flip-flop using SR Flip-Flop.	5	K1	CO3
		ii.	Explain the working philosophy of a 3-bit universal shift register with a neat sketch.	8	K2	CO3
14.	a)		An asynchronous sequential circuit is described by the following excitation and output function, $Y = X_1X_2 + (X_1 + X_2)Y$ and $Z = Y$.		K3	CO4
		i.	Draw the logic diagram of the circuit.	5		
		ii.	Derive a transition table, flow table and output map and describe the behavior of the circuit.	8		
			(OR)			
	b)		Discuss the various types of hazard. How to design a hazard free circuits, explain with example?	13	K1	CO4

15.	a)	Why it is necessary to use a ROM in personal computers? Explain various types of ROM in detail.	13	K2	CO5
		(OR)			
	b)	Explain in detail about the Programmable Logic Array (PLA), Programmable Array Logic (PAL) and Field Programmable Gate Arrays (FPGA).	13	K2	CO5

PART – C

(1 x 15 = 15 Marks)

Q.No.		Questions	Marks	KL	CO
16.	a)	Design a BCD to Excess-3-code converter using minimum number of NAND gates.	15	K3	CO2
		(OR)			
	b)	Design a counter using JK flip-flops with a following binary sequence: 1, 2, 5, 7 and repeat.	15	K3	CO3